### PAL Timing

<table>
<thead>
<tr>
<th>phi1</th>
<th>phi2</th>
<th>BDIR</th>
<th>BC1</th>
<th>BC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>valid</td>
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</tr>
</tbody>
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#### Notes:
- BC1, BC2 delayed approx 20 us due to additional levels of TTL logic on those paths. Must treat as skew due to asymmetric TTL switching behavior, and the fact Inty 2 has a dedicated chip for this that may reduce the differential delay on these paths.

#### Sampling sequence
- Offset 0--early exit
- Offset 1--early exit
- Offset 2--early exit
- Offset 1--late exit
- Offset 2--late exit

### NTSC Timing

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#### Sampling sequence
- Offset 0--early exit
- Offset 1--early exit
- Offset 2--early exit
- Offset 0--late exit
- Offset 1--late exit
- Offset 2--late exit